Paper No. 21

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte NARUMI SAKASHITA and KAZUTAMI ARIMOTO

Appeal No. 1999-1098
Application 08/627,313

ON BRIEF

Before THOMAS, HAIRSTON, and FLEMING, ***Administrative Patent Judges***.

FLEMING, ***Administrative Patent Judge***.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 1-13, all of the claims pending in the present application.

The instant invention relates generally to semiconductor memory devices with arrangements of memory blocks and peripheral circuits (specification, page 1, lines 6-9).

Specifically, the memory blocks (figure 1, B1-B64) are arranged on a semiconductor substrate (10) to surround peripheral circuits (11-14) which are situated at the center of each unit block (U1-U4). Each memory block includes a plurality of word lines (figure 2, item 17), a plurality of bit lines (figure 2, item 18, 19) crossing the word lines, and a plurality of memory cells (figure 2, item 20) each corresponding to a crossing point of the word line and the bit line.

Multiple embodiments are disclosed (figures 6-13).

Appellants' independent claims 1 and 13, reproduced below, are representative of the invention:

1. A semiconductor memory device, comprising:

a semiconductor substrate;

a plurality of memory blocks, each memory block having an outer peripheral boundary delineating an entire area of the memory block with each memory block including a plurality of word lines, a plurality of bits lines crossing said plurality of word lines, and a plurality of memory cells corresponding to crossing points of said plurality of word lines and said plurality of bit lines positioned within the entire area of the memory block, a portion of the outer peripheral boundary of said each memory block corresponding to a portion of the outer peripheral boundary of each adjacent memory block, said plurality of memory blocks being arranged on said semiconductor substrate to completely surround a center of said semiconductor substrate; and

a peripheral circuit for said plurality of memory blocks arranged on said semiconductor substrate at a center of said memory blocks, completely surrounded by said plurality of memory blocks.

13. A semiconductor memory device comprising:

a semiconductor substrate;

first through fourth memory blocks arranged on said semiconductor substrate to surround a center of said semiconductor substrate, each memory block having a rectangular shape and including a plurality of word lines, a plurality of bit lines crossing said plurality of word lines, and a plurality of memory cells corresponding to crossing points of said plurality of word lines and said plurality of bit lines; and

a peripheral circuit for said first through fourth memory blocks, disposed on said semiconductor substrate at a center of said first through fourth memory blocks; wherein

said first memory block is arranged so that one shorter side of said first memory block is adjacent to one longer side of said fourth memory block and one longer side of said first memory block is located on an extension of one shorter side of said fourth memory block,

said second memory block is arranged so that one shorter side of said second memory block is adjacent to another longer side of said first memory block and one longer side of said second memory block is located on an extension of another shorter side of said first memory block,

said third memory block is arranged so that one shorter side of said third memory block is adjacent to another longer side of said second memory block and one longer side of said third memory block is located on an extension of another shorter side of said second memory block, and

said fourth memory block is arranged so that another shorter side of said fourth memory block is adjacent to another longer side of said third memory block and another longer side of said fourth memory block is located on an extension of another shorter side of said third memory block.

In rejecting Appellants' claims, the Examiner relies on Appellants' admitted prior art and the following references:

Seefeldt et al. (Seefeldt)	4,864,381	Sep. 5, 1989
Ichiguchi	5,222,042	Jun. 22, 1993
Koike	5,229,629	Jul. 20, 1993
Katto et al. (Katto)	5,416,347	May 16, 1995
Kusunoki et al. (Kusunoki)	5,512,766	Apr. 30, 1996

Claims 1-12 stand rejected under 35 U.S.C. § 103(a) as being obvious over the admitted prior art and Kusunoki and Seefeldt. Claim 10 stands rejected under 35 U.S.C. § 103(a) as being obvious over the admitted prior art, Kusunoki, Seefeldt and Ichiguchi.

Claim 12 stands rejected under 35 U.S.C. § 103(a) as being obvious over the admitted prior art, Kusunoki, Seefeldt and Katto.

Claim 13 stands rejected under 35 U.S.C. § 103(a) as being obvious over the admitted prior art, Kusunoki, Seefeldt and Koike.

Rather than repeat the arguments of Appellants and the Examiner, we refer the reader to the Appellants' Briefs[1] and Examiner's Answer[2] for the respective details thereof.

OPINION

With full consideration being given the subject matter on appeal, the Examiner's rejection and the arguments of Appellants and the Examiner, for the reasons stated **infra**, we will reverse the Examiner's rejection of claims 1-12 under 35 U.S.C. § 103(a) as being unpatentable over the combinations of the admitted prior art, Kusunoki, and Seefeldt.

In rejecting claims under 35 U.S.C. § 103, the Examiner bears the initial burden of establishing a ***prima facie*** case of

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[1] Appellants filed a Brief on August 27, 1997. Appellants subsequently filed a Reply Brief on November 17, 1997.

[2] The Examiner, in response to Appellants' Brief, mailed an Examiner's Answer on October 8, 1997.

obviousness. ***In re Oetiker***, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992). The Examiner can satisfy this burden only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references. ***In re Fine***, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598. Only if this initial burden is met does the burden of coming forward with evidence or argument shift to the Appellants. ***Oetiker***, 977 F.2d at 1445, 24 USPQ2d at 1444. ***See also In re Piasecki***, 745 F.2d 1468, 1472, 223 USPQ 785, 788 ("After a ***prima facie*** case of obviousness has been established, the burden of going forward shifts to the applicant."). If the Examiner fails to establish a ***prima facie*** case, the rejection is improper and accordingly merits reversal. ***Fine***, 837 F.2d at 1074, 5 USPQ2d at 1598.

An obviousness analysis commences with a review and consideration of all the pertinent evidence and arguments. ***See Oetiker***, 977 F.2d at 1445, 24 USPQ2d at 1444 ("In reviewing the examiner's decision on appeal, the Board must

necessarily weigh all of the evidence and argument."). Accordingly, we now consider the claims on appeal.

Appellants first point out[3] that their admitted prior art describes the disadvantages associated with the prior art and Appellants' claims clearly distinguish over this prior art. Next, Appellants summarize[4] that the Kusunoki reference describes the use of memory mats and mat periphery circuits which correspond to the memory blocks and the peripheral circuit recited in claim 1. However, Appellants assert that the periphery circuits of Kusunoki are not located at the center of the memory mats as required by claim 1.

As regards Seefeldt, Appellants argue[5] that it is clear legal error for the Examiner not to address the differences between the claimed semiconductor memory device having a plurality of memory blocks and a peripheral circuit, and the gate array arrangement of Seefeldt. Appellants further argue that since none of the applied prior art references suggests

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[3] Brief, page 9

[4] Brief, pages 9-10

[5] Brief, page 11

the specific arrangement of memory blocks and peripheral circuits as claimed, and such arrangement addresses a particular need in the art (providing substantially equal signal delay between the peripheral circuit and the respective memory blocks), the actual motivation for the Examiner's proposed modification of the prior art to arrive at the claimed invention is found in Appellants' disclosure.

As regards prior art figure 17, Appellants argue[6] that while a peripheral circuit might be interpreted to be located at the center of the semiconductor substrate, it is not completely surrounded by memory blocks since there are openings between memory blocks MA1-MA4.

In addition, Appellants assert[7] that the Examiner's sole basis as to why one skilled in the art would have been led by the prior art as a whole to modify or combine the applied prior art to arrive at the claimed invention is that it is a simple design choice to arrange the cells and peripheral circuits. This basis, Appellants argue, is not a logical

[6] Brief, page 9

[7] Brief, page 14

reason why one having ordinary skill in the art would have been motivated to modify prior art figures 16-17 in view of Kusunoki and Seefeldt to arrive at the claimed invention.

The Examiner asserts[8] that prior art figures 16 and 17 teach all the claimed structure except for the word lines and bit lines, and that Kusunoki teaches word and bit lines. The Examiner then cites Seefeldt as teaching I/O peripheral circuits intermingled with gate memory blocks wherein the I/O peripheral circuits reside at the center of radially formed blocks. The Examiner then finds "It would have been obvious to a skilled artisan to apply the teachings of Kusunoki and Seefeldt as a simple design choice for arrangement of the cells and periphery therein."

In regard to Appellants' argument that the openings shown in prior art figures 16-17 do not meet the "completely surrounded" limitation, the Examiner asserts[9] that the openings are merely block diagram illustrations from one memory cell array to the next. The Examiner further asserts

[8] Answer, page 4

[9] Answer, page 7

that these figures are no different from the cover figure of Kusunoki which shows no spacing between the arrays, and that when looking at a real layout, such as figures 9-11, the spacing is made as small as possible (Examiner's emphasis) in accordance with known semiconductor design rules.

In addition, the Examiner asserts[10] that the claim language "completely surrounded" is met by the block diagram shown in figure 17, as memory cells reside at all sides around the peripheral circuit and thus surround the peripheral circuit. The Examiner further states "in the Examiner's opinion, wiring layers also comprise the memory circuits and since wiring layers traverse the "gaps," the peripheral circuit is clearly "completely surrounded."

Finally, the Examiner refers[11] to Seefeldt as showing I/O cells, or peripheral cells, at the center of other circuitry.

As pointed out by our reviewing court, we must first determine the scope of the claim. "[T]he name of the game is

[10] Answer, page 7

[11] Answer page 8

the claim." ***In re Hiniker Co.***, 150 F.3d 1362, 1369, 47 USPQ2d 1523, 1529 (Fed. Cir. 1998).

Claim one recites,[12]

> said plurality of memory blocks being arranged on said semiconductor substrate to completely surround a center of said semiconductor substrate; and
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> a peripheral circuit for said plurality of memory blocks arranged on said semiconductor substrate at a center of said memory blocks, completely surrounded by said plurality of memory blocks.

We first turn to the Examiner's finding that the claim language "completely surrounded" is met by the block diagram shown in figure 17, as memory cells reside at all sides around the peripheral circuit and thus surround the peripheral circuit. We disagree, as it is clear from this figure that there are no memory blocks at the sides of the peripheral circuit, only above and below it. To completely surrounded the peripheral circuit with memory blocks as claimed, the memory blocks must simultaneously extend on all sides of the peripheral circuit so as to enclose or confine it. It is clear from figure 17 that this is not the case.

[12] Lines 12-17

As regards the Examiner's argument that in a real layout the spacing is made as small as possible in accordance with known semiconductor design rules, we nevertheless find that as there are no memory blocks at the right and left sides of the peripheral circuit of figure 17, it is not completely surrounded.

Turning to Seefeldt we find that this reference teaches I/O peripheral circuits (32) intermingled with gate circuits (31) wherein the I/O peripheral circuits reside at the center of radially formed blocks. However, we find that Seefeldt is replete with teachings[13] to intermingle or interdistribute gate cells and I/O cells rather than surrounding the gate cells with the I/O cells. Furthermore, the reason given[14] by Seefeldt for the intermingling is the improved routability caused by locating the I/O cells close to the circuitry that have been routed to perform a prescribed circuit function. This is done to reduce interconnects between the cells and global routing channels. This is not a reason to completely

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[13] Column 2, lines 5-9; column 3, lines 46-62; column 5 lines 16-26 and 40-57; column 6, lines 4-14

[14] Column 6, lines 14

surround I/O cells with gate cells, but to interdisperse the cells. Appellants' invention requires that the memory blocks surround the peripheral circuit in order to provide substantially equal signal delay between the peripheral circuit and the respective memory blocks.

Finally, we find in the Examiner's conclusion that it would have been obvious to a skilled artisan to apply the teachings of Kusunoki and Seefeldt as a simple design choice for arrangement of the cells and periphery, to be without evidentiary basis. As Appellants' specification clearly presents[15] the reason for the claimed arrangement, i.e., to reduce unequal signal delays due to different path lengths, the Examiner must provide evidence why one of ordinary skill in this art would have selected the claimed arrangement of memory blocks and peripheral circuits.

Similarly, as regards claim 8, the Examiner finds[16] "It would have been obvious to a skilled artisan to apply the teachings of Kusunoki and Seefeldt as a simple design choice

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[15] Page 14, lines 14-17

[16] Answer, page 4

for arrangement of the cells and periphery therein." (Emphasis added). Hereto, as Appellants have provided a reason for the claimed arrangement, i.e., to reduce unequal signal delays due to different path lengths, the Examiner must provide evidence as to why one of ordinary skill in this art would have selected the claimed arrangement of memory blocks and peripheral circuits. No such evidence is of record.

Finally, as regards claim 13, the Examiner adds the Koike reference and notes[17] that it provides for an arrangement of blocks wherein the long sides of one block are adjacent short sides of another block. The Examiner then finds "It would have been obvious to a skilled artisan to combine the teachings of Koike with the Prior Art Figs. 16-17, Kusunoki and Seefeldt as a choice in design in order to optimize space on the wafer as clearly taught by Koike."

First, we find that Koike provides[18] the particular circuit placement in order to reduce the minimum distance between the terminals of the cells, a purpose different from

[17] Answer, page 6

[18] Column 4, lines 7-13

that of Appellants. This purpose does not provide any reason to one skilled in the art to provide the claimed[19] memory blocks to surround the peripheral circuit.

The Federal Circuit states that "[t]he mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." ***In re Fritch***, 972 F.2d 1260, 1266 n.14, 23 USPQ2d 1780, 1783-84 n.14 (Fed. Cir. 1992), ***citing In re Gordon***, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984). "Obviousness may not be established using hindsight or in view of the teachings or suggestions of the inventor." ***Para-Ordnance***, 73 F.3d at 1087, 37 USPQ2d at 1239, ***citing W. L. Gore & Assocs.***, 721 F.2d 1551, 1553, 220 USPQ 311, 312-13. In addition, our reviewing court requires the PTO to make specific findings on a suggestion to combine prior art references. ***In re Dembiczak,*** 175 F.3d 994, 1000-01, 50 USPQ2d 1614, 1617-19 (Fed. Cir. 1999). ***In re Lee,*** 277 F.3d 1338, 1343, 61 USPQ2d 1430, 1433-34 (Fed. Cir. 2002).

[19] Lines 3-12

As regards claim 10, the Examiner adds the Ichiguchi reference solely for its teaching of peripheral circuits including address strobe buffering, read buffers, write buffers and row and column decoders. As regards claim 12, The Examiner adds the Katto reference solely for its teaching of redundancy circuitry in memory cell arrays for correction of bad cells. As these references are not relevant to our decision above, the rejection of these dependent claims is reversed for the reasons given above.

Therefore, based on the foregoing, we conclude that the Examiner has failed to establish a ***prima facie*** case of unpatentability under 35 U.S.C. § 103 with respect to claims 1-13.

Accordingly, we reverse the Examiner's rejection of claims 1-12 under 35 U.S.C. § 103(a) as obvious over the admitted prior art and Kusunoki and Seefeldt; the rejection of claim 10 under
35 U.S.C. § 103(a) as obvious over the admitted prior art, Kusunoki, Seefeldt and Ichiguchi; the rejection of claim 12 under 35 U.S.C. § 103(a) as obvious over the admitted prior

art, Kusunoki, Seefeldt and Katto; and the rejection of claim 13 under 35 U.S.C. § 103(a) as obvious over the admitted prior art, Kusunoki, Seefeldt and Koike.

REVERSED

JAMES D. THOMAS Administrative Patent Judge	)	
KENNETH W. HAIRSTON Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
MICHAEL R. FLEMING Administrative Patent Judge	)	

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